Notice of Allowability	Application No.	Applicant(s)	
	09/733,686	GOLDOVSKY, ALEXANDER	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/05/2004*.

2. ☒ The allowed claim(s) is/are *1,2 and 4-17*.

3. ☒ The drawings filed on *08 December 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *02/02/2005* .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Joseph B. Ryan on 02/02/2005.

The application has been amended as follows:

Re claim 1, as recommended by the applicant for further defining the transmit signal and generate signal are t_{n-1} and g_{n-1} of the n-bit adder, the examiner amends claim 1 as:

An adder comprising: a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated utilizing a transmit signal and a generate signal of the adder; wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder, and wherein the transmit

signal and generate signal are (n-1)th transmit signal and (n-1)th generate signal respectively of the n-bit adder.

Re claim 6, as recommended by the applicant for further defining the structure of the multiplexer, the examiner amends claim 6 as:

An adder comprising: a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder, and a flag generation circuit coupled to a plurality of signal lines of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder; wherein the flag generation circuit comprises a multiplexer ~~having at least a first input coupled to a first one of the plurality of signal lines, a second input coupled to a second one of the plurality of signal lines~~ having at least a first input corresponding to a transmit signal coupled to a first one of the plurality of signal lines, a second input corresponding to a generate signal coupled to a second one of the plurality of signal lines, a select signal input coupled to a third one of the plurality of signal lines, and an output, the multiplexer being configured to select one of a plurality of input signals applied to its first and second inputs for propagation to its output as the overflow flag based at least in part on a signal applied to the select signal input.

Re claim 7, as recommended by the applicant for further defining the structure of the multiplexer, the examiner amends claim 7 as:

An adder comprising: a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and a flag generation circuit coupled to a plurality of signal lines of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder; wherein the flag generation circuit comprises a 2-to-1 multiplexer ~~having a first input coupled to a first one of the plurality of signal lines and having a first signal applied thereto, a second input coupled to a second one of the plurality of signal lines~~ having a first input corresponding to a transmit signal coupled to a first one of the plurality of signal lines and having a first signal applied thereto, a second input corresponding to a generate signal coupled to a second one of the plurality of signal lines and having a second signal applied thereto, an output corresponding to the overflow flag, and a select signal input coupled to a third one of the plurality of signal lines for selecting one of the first signal and the second signal for propagation to the output as the overflow flag.

Re claim 16, the examiner amends claim 16 as:

An integrated circuit comprising: at least one adder, the adder comprising: (i) a plurality of computational stages each associated with one or more bit positions of the

adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder; and (ii) a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated utilizing a transmit signal and a generate signal of the adder; wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder, and wherein the transmit signal and generate signal are (n-1)th transmit signal and (n-1)th generate signal respectively of the n-bit adder.

Re claim 17, the examiner amends claim 17 as:

A method for performing a computational operation in an adder, the method comprising the steps of: providing a plurality of computational stages each associated with one or more bit positions of the adder, the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder, and generating an overflow flag for the adder using at least one signal associated with at least one of the computational stages, the overflow flag being separate and distinct from the primary carry-output signal, the overflow flag being generated utilizing a transmit signal and a generate signal of the adder; wherein the adder comprises an n-bit adder and the primary carry-output signal comprises a primary carry-output signal c_{n-1} of the n-bit adder, and wherein the transmit

signal and generate signal are (n-1)th transmit signal and (n-1)th generate signal respectively of the n-bit adder.

2. Claims 1-2 and 4-17 are allowed.

3. Claim 3 is cancelled.

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or renders an obviousness of an adder comprising a plurality of computational stages and a flag generation circuit coupled to at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being separate and distinct from the primary carry-output signal c_{n-1} of the n-bit adder and the overflow flag being generated utilizing a (n-1)th transmit signal and a (n-1)th generate signal of the n-bit adder as cited in independent claims 1, 5, and 16-17 wherein the flag generation circuit further comprising a multiplexer coupled to the transmit signal and generate signal to output an overflow flag as cited in claims 6-8.

The closest found prior art is Rim (U.S. 5,907,498). Rim discloses an adder comprising a plurality of computational stages and a flag generation circuit coupled to at least one of the computational stages and operative to generate an overflow flag for the adder wherein the overflow flag being separate and distinct from the primary carry-output signal of the n-bit adder. However, Rim fails to disclose the overflow flag being generate utilizing a (n-1)th transmit signal and a (n-1)th generate signal of the n-bit adder or the multiplexer coupled to the transmit signal and generate signal to output an overflow flag.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

February 21, 2005

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